AMENDMENTS TO THE CLAIMS

Please amend claims 1, 3-4, 6-8, and 11-12;

Please cancel claim 13 without prejudice or disclaimer; and

Please add new claims 14-20 as follows:

1. (currently amended) An input and output driver comprising:

an input buffer for supplying an input data from a DQ pad to a memory cell array in a writing mode;

an output driver for supplying an output data from the memory cell array to the DQ pad in a reading mode; and

a DQ switch electrically connected between the output driver and the DQ pad, ~~for~~ the DQ switch electrically isolating the output driver from the DQ pad in the writing mode and electrically connecting the output driver to the DP pad in the reading mode.

2. (original) An input and output driver according to claim 1, wherein the DQ switch comprises an NMOS transistor or a PMOS transistor.

3. (currently amended) An input and output driver according to claim 1, wherein the DQ switch comprises ~~an LVT~~ a low threshold voltage NMOS transistor or ~~an LVT~~ a low threshold voltage PMOS transistor.

4. (currently amended) An input and output driver according to claim 1, wherein the DQ switch comprises at least two ~~LVT~~ low threshold voltage NMOS transistors or at least two ~~LVT~~ low threshold voltage PMOS transistors connected in parallel.

5. (original) An input and output driver according to claim 1, wherein the DQ switch is a transfer gate.

6. (currently amended) An input and output driver according to claim 5, wherein the transfer gate comprises ~~an LVT~~ a low threshold voltage NMOS transistor and ~~an LVT~~ a low threshold voltage PMOS transistor connected in parallel.

7. (currently amended) An input and output driver according to claim 6, wherein the ~~LVT~~ low threshold voltage NMOS transistor is operated by a pumping voltage or a power source voltage.

8. (currently amended) An input and output driver according to claim 6, wherein the ~~LVT~~ low threshold voltage PMOS transistor is operated by a negative pumping voltage or a ground voltage.

9. (original) An input and output driver according to claim 1, wherein the DQ switch is operated by a pumping voltage higher than a power source voltage.

10. (original) An input and output driver according to claim 1, wherein a total capacitance of the DQ switch is smaller than that of the output driver.

11. (currently amended) An input and output driver according to claim 1, further comprising an ~~ODT~~ on-die termination circuit connected between a power source voltage and a node to which the DQ switch and the DQ pad are connected.

12. (currently amended) An input and output driver according to claim 1, further comprising an ~~ESD~~ electrostatic discharge protection circuit and a ~~CDM~~ charged device mode circuit connected between the input buffer and the DQ pad.

13. (canceled)

14. (new) An input and output driver comprising:

an input buffer for supplying an input data from a DQ pad to a memory cell array in a writing mode;

an output driver for supplying an output data from the memory cell array to the DQ pad in a reading mode;

a DQ switch connected between the output driver and the DQ pad, the DQ switch electrically isolating the output driver from the DQ pad in the writing mode and electrically connecting the output driver to the DQ pad in the reading mode;

an on-die termination circuit connected between a power source voltage and a node to which the DQ switch and the DQ pad are connected; and

an electrostatic discharge protection circuit connected between the input buffer and the DQ pad.

15. (new) The input and output driver according to claim 14, wherein the DQ switch comprises a low threshold voltage NMOS transistor or a low threshold voltage PMOS transistor.

16. (new) The input and output driver according to claim 14, wherein the DQ switch comprises at least two low threshold voltage NMOS transistors or at least two low threshold voltage PMOS transistors connected in parallel.

17 (new) The input and output driver according to claim 14, wherein the DQ switch is a transfer gate.

18 (new) The input and output driver according to claim 14, wherein the DQ switch is operated by a pumping voltage higher than a power source voltage.

19 (new) The input and output driver according to claim 14, wherein a total capacitance of the DQ switch is smaller than that of the output driver.

20 (new) The input and output driver according to claim 14, further comprising a charged device model circuit connected between the electrostatic discharge protection circuit and the input buffer.